

Turbo Chameleon

VGA, turbo, freezer and memory expansion for the Commodore-64
(Also standalone C64 mode and C-One core)

The Programmers Manual

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Contents

1	Introducing the Chameleon core	2
1.1	Turbo Chameleon Cartridge for the C64	2
1.2	Standalone Mode	2
1.3	Chameleon core for the C-One Reconfigurable Computer	2
2	Configuration Mode	2
2.1	Detecting a Chameleon	2
2.2	Activating Configuration Mode	3
2.3	Configuration Registers	3
3	Memory	5
3.1	Memory Bank Layout	5
3.1.1	16 MByte Layout	5
3.1.2	32 MByte Layout	5
3.2	Bank Switching Registers	6
3.3	Memory Windows	7
4	VGA Output	7
4.1	VGA Resolution and Sync Registers	7
4.2	Example settings for standard VGA modes	8
4.3	Chameleon Object Processor	8
4.4	Palette Registers	10
4.5	Fixed Palette Entries	10
5	REU (Ram Expansion Unit) Emulation	10
5.1	REU Registers	10
5.2	Blitter extension	11
6	CPU Turbo/Accelerator	12
7	Disk Drive Emulation	12
8	Complete register map	12

1 Introducing the Chameleon core

The Turbo Chameleon FPGA core can run in a few different configurations and so can be used in various ways. The Chameleon cartridge itself can also run other cores. This documentation however only covers the C64 mode of the cartridge.

1.1 Turbo Chameleon Cartridge for the C64

This is the main purpose of the core and also where the name 'Chameleon' is coming from. It can emulate various cartridges and peripherals in a way that is invisible to the software. Most of the functions of the original C64 hardware is taken over by an enhanced emulation in the cartridge. This gives access to all data and address lines, but also internal registers and various control signals normally not accessible on the cartridge port. The CPU can be made to run faster, memory is expanded and various cartridges can be mapped into the address space without changing anything to the main machine.

1.2 Standalone Mode

1.3 Chameleon core for the C-One Reconfigurable Computer

Both the Chameleon cartridge and the C-One extender board are based on the same type of FPGA. Therefore it made sense to release a Chameleon core for the C-One with extender board. The C-One version of Chameleon behaves like the standalone mode of the Chameleon Cartridge. Because the hardware is different there are some small differences between the two cores. The most important difference are in the amount of memory available and the layout of the memory map.

2 Configuration Mode

Configuration mode is where the required functionality is selected and additional registers and extensions are switched on. The configuration registers are located at 53488 ($D0F0_h$) to 53503 ($D0FF_h$). It is recommended to deactivate configuration mode after the required settings have been made, as some programs could overwrite these registers by accident.

2.1 Detecting a Chameleon

Because the Chameleon can emulate a variety of cartridges and even combinations of those, the normal cartridge type detection method by probing DE_{xx_h} or DF_{xx_h} fails to reliably detect it. However if the Chameleon is active, a few extra registers are visible in one of the VIC-II mirror areas. Reading at address 53502 ($D0FE_h$) on a stock machine always results in 255 (FF_h). On the Chameleon the value is unequal to 255 (FF_h) if configuration mode is active. Use the following sequence to reliably detect the presence of the Chameleon: Read and backup the current value at 53502. Write 42 ($2A_h$) at 53502 ($D0FE_h$) and read at the same location. The value represents the FPGA core version. If the backup value was 255 (FF_h) store it into 53502 ($D0FE_h$) to restore previous mode.

Core version number	Configuraion or Mode
1 01_h	C64 with Chameleon cartridge present
161 $A1_h$	Chameleon running in standalone mode (C64 emulation)
193 $C1_h$	Chameleon core for the C-One reconfigurable computer
255 FF_h	C64 without Chameleon

2.2 Activating Configuration Mode

To enter configuration mode and make the setup registers available write the value 42 ($2A_h$) in memory location 53502 ($D0FE_h$). To disable the configuration registers write 255 (FF_h) at this location. Any value written to either 53501 ($D0FD_h$) or 53503 ($D0FF_h$) also leaves configuration mode. Activation of configuration mode is very unlikely to happen by accident as sequential writes will never or only briefly activate the registers. During configuration mode the extra registers are visible from 53488 ($D0F0_h$) to 53503 ($D0FF_h$). With these registers other memory areas can be configured and additional registers mapped into the CPU address space.

2.3 Configuration Registers

Address (Hex)	Address (Dec)	Name	Description
$D0F0_h$	53488	CFG???	Reserved
$D0F1_h$	53489	CFG???	Reserved
$D0F2_h$	53490	CFGVIC	VIC-II Emulation Config
	bit settings		description
	7	VIC-II Read Enable	0 = Off 1 = Perform memory accesses for VIC-II
	6-5	VIC-II update framebuffer	00 = No update, there is no output from VIC-II on the VGA 01 = VIC-II writes to VGA framebuffer at 2097152-2228223 ($200000_h-21FFFF_h$) 10 = VIC-II writes to VGA framebuffer at 4194304-4325375 ($400000_h-41FFFF_h$) 11 = VIC-II writes to VGA framebuffer at 6291456-6422527 ($600000_h-61FFFF_h$)
	4	reserved, must be 0	-
	3	VIC-II emulation error (or hardware problem)	0 = VGA emulation in sync. with VIC-II chip 1 = Error, VGA and VIC-II chip not in sync. This bit is read-only and has a value in cartridge mode only.
	2-0	VIC-II type	000 = PAL (63 columns, 312 lines) 001 = Reserved 010 = NTSC (65 columns, 263 lines) 011 = Old-NTSC (64 columns, 262 lines) 1xx = Reserved These bits are read-only in cartridge mode. They can be changed in standalone mode and on the C-One.
$D0F3_h$	53491		Reserved
$D0F4_h$	53492	CFGTUR	Turbo configuration
	bit settings		description
	7	Turbo Enable	0 = 1 Mhz mode 1 = Turbo mode active
	6	Turbo switch	0 = Manual setting 1 = Turbo mode is switchable
	5	VIC-II turbo bit	0 = Off 1 = "Turbo Enable" is mirrored at bit 0 of $D030_h$
	4-0	reserved, must be 0	-
$D0F5_h$	53493		Reserved
$D0F6_h$	53494	CFGREU	REU (Ram Expansion Unit) Emulation Config
	bit settings		description
	7	1 = Enable REU	Enable REU emulation and activate registers at $DF00_h-DF0A_h$.
	6	1 = Enable Blitter Extensions	Extra registers are added at $DF0B_h-DF0F_h$ that enhance the REU so it can perform simple bit-bit functions.
	5	reserved, must be 0	-
	4	reserved, must be 0	-
	3	reserved, must be 0	-
	2-0	REU memory size	000 = 128 KByte 001 = 256 KByte 010 = 512 KByte 011 = 1 MByte 100 = 2 MByte 101 = 4 MByte 110 = 8 MByte 111 = 16 MByte (Not available on C-One, selects 8 MByte)

D0F7 _h	53495	CFGCIA	CIA, keyboard and IEC configuration
bit	settings	description	
7	IEC port	0 = Chameleon IEC bus connected to virtual CIAs 1 = Chameleon IEC bus is disconnected By setting this bit, the Chameleon IEC bus is disconnected from the C64 side. In this mode the Chameleon can function as a 1541 drive emulator. This feature is not available on the C-One due to a hardware limitation.	
6-2	Reserved		
1	CIA-2 emulation	0 = Old 1 = Type A This bit has no effect in cartridge mode	
0	CIA-1 emulation	0 = Old 1 = Type A This bit has no effect in cartridge mode	
D0F8 _h	53496	CFGFD0	Drive emulation
bit	settings	description	
7	Enable virtual-drive CPU	0 = drive cpu stopped 1 = drive cpu running	
6	Reset virtual-drive CPU	0 = normal operation 1 = drive reset (bit 7 must be 1 for proper reset)	
5-2	Reserved, must be 0	-	
1-0	Drive ID jumpers	00 = drive device id is 8 01 = drive device id is 9 10 = drive device id is 10 11 = drive device id is 11	
D0F9 _h	53497	CFGFD1	Reserved for second drive
bit	settings	description	
7	Enable virtual-drive CPU	0 = drive cpu stopped 1 = drive cpu running	
6	Reset virtual-drive CPU	0 = normal operation 1 = drive reset (bit 7 must be 1 for proper reset)	
5-2	Reserved, must be 0	-	
1-0	Drive ID jumpers	00 = drive device id is 8 01 = drive device id is 9 10 = drive device id is 10 11 = drive device id is 11	
D0FA _h	53498	CFGREG	Enable VGA, palette and window registers
bit	settings	description	
7	Enable memory window at D7xx _h	0 = standard function (SID mirror) 1 = Memory window	
6	Enable memory window at D6xx _h	0 = standard function (SID mirror) 1 = Memory window	
5	Enable memory window at D5xx _h	0 = standard function (SID mirror) 1 = Memory window	
4	reserved, must be 0	-	
3	Palette Registers Enable	0 = VIC-II chip mirrors at D100 _h -D3FF _h 1 = Palette registers are at D100 _h -D3FF _h	
2	Enable Bank Registers	0 = VIC-II chip mirrors at D0B0 _h -D0BF _h 1 = Bank and MMU at D0B0 _h -D0BF _h	
1	Enable memory window address registers	0 = VIC-II chip mirrors at D0A0 _h -D0AF _h 1 = Memory window addresses at D0A0 _h -D0AF _h	
0	Enable VGA Controller Registers	0 = VIC-II chip mirrors at D040 _h -D07F _h 1 = VGA registers at D040 _h -D07F _h	
D0FB _h	53499	CFGBOT	Boot control register
bit	settings	description	
7	Boot Image	If bit 7 of this register is zero, a special bootrom contained in the FPGA image is mapped to E000 _h -FFFF _h or 8000 _h -9FFF _h depending on cartridge revision. This bootrom is responsible for initializing the cartridge at power-up. 0 = Bootrom mapped into C64 memory space 1 = Normal operation	
6	ROM source	0 = C64 original Basic and Kernal ROMs are used 1 = All memory and ROMs are banked with D0B0 _h -D0BF _h This bit is only functional in cartridge mode. In standalone mode and on the C-One this bit should always be set. Note that the character ROM is always emulated and never the C64 original.	
5-0	reserved, must be 0	-	
D0FC _h	53500	CFG???	Reserved
D0FD _h	53501	CFGDIS	A write (any value) leaves configuration mode
D0FE _h	53502	CFGENA	Write 42 (2A _h) to enter configuration mode
D0FF _h	53503	CFGDIS	A write (any value) leaves configuration mode

3 Memory

The Chameleon Cartridge brings its own memory. The internal memory of the C64 will not be used except for the color ram. Because the CPU and VIC-II chip can only access 64 Kbyte at a time, a few tricks are required to address more. There are different methods implemented, so the best one can be chosen for each purpose.

By far the fastest method to move data around in memory is using the REU. If the blitter extensions are activated the REU can access any byte in the full memory range. In compatible mode it is limited to a range of upto 16 Mbyte in REU space and 64 Kbyte in the CPU space. Bank switching is available for banking in pages from the first 2 Mbyte into CPU space. This gives support for ROM replacements, ROM cartridge emulation and even multitasking. Not all pages are available as some are reserved for the Chameleon firmware. For accessing beyond 2 Mbyte upto three memory windows can be activated. These memory windows give access to the full memory range, but only with 256 bytes at a time.

The CPU is not the only device using memory. The REU emulation was already mentioned, which has upto 16 Mbyte of internal storage in REU mode. The drive emulation needs storage space for the disk images. Also the VGA video port uses quite a bit of framebuffer memory.

3.1 Memory Bank Layout

3.1.1 16 MByte Layout

This is the memory layout used by the C-One Chameleon core. The C-One extender board has 16 MByte of memory.

Address (Hex)	Address (Dec)	Name	Description
00 0000 _h -00 FFFF _h			64 KByte RAM for C64 mode
01 0000 _h -0F FFFF _h			960 Kbyte RAM free for user programs
10 0000 _h -10 FFFF _h			Kernal and Basic rom images
11 0000 _h -11 FFFF _h			Additional rom images
12 0000 _h -12 FFFF _h			Drive CPU emulation (first device)
13 0000 _h -13 FFFF _h			Reserved for second drive
14 0000 _h -17 FFFF _h			256 KByte for cartridge emulation (RetroReplay, FinalCartridge)
18 0000 _h -1F FFFF _h			512 KByte for Chameleon OS and libraries
20 0000 _h -3F FFFF _h			2 MByte for disk images
40 0000 _h -7F FFFF _h			4 Mbyte video RAM
80 0000 _h -FF FFFF _h			8 MByte REU memory

3.1.2 32 MByte Layout

This is the memory layout used by the Turbo Chameleon Cartridge both as cartridge and in standalone mode.

Address (Hex)	Address (Dec)	Name	Description
000 0000 _h -000 FFFF _h			64 KByte RAM for C64 mode
001 0000 _h -00F FFFF _h			960 Kbyte RAM free for user programs
010 0000 _h -010 FFFF _h			Kernal and Basic rom images
011 0000 _h -011 FFFF _h			Additional rom images
012 0000 _h -012 FFFF _h			Drive CPU emulation (first device)
013 0000 _h -013 FFFF _h			Reserved for second drive
014 0000 _h -017 FFFF _h			256 KByte for cartridge emulation (RetroReplay, FinalCartridge)
018 0000 _h -01F FFFF _h			512 KByte for Chameleon OS and libraries
020 0000 _h -03F FFFF _h			2 MByte for disk images
040 0000 _h -0FF FFFF _h			12 Mbyte video RAM
100 0000 _h -1FF FFFF _h			16 MByte REU memory

3.2 Bank Switching Registers

The banking registers give the CPU access to the first 2Mbyte of memory. Each 8 Kbyte block can be mapped inside this 2 Mbyte range in steps of 8K. This includes kernal, basic and character ROMS. Simple cartridge emulation (8KByte @ 8000_h) is available as there are separate read and write registers for the 8000_h to 9FFF_h range.

Address (Hex)	Address (Dec)	Name	Description
D0B0 _h		BNK00	0000 _h –1FFF _h RAM
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B1 _h		BNK20	2000 _h –3FFF _h RAM
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B2 _h		BNK40	4000 _h –5FFF _h RAM
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B3 _h		BNK60	6000 _h –7FFF _h RAM
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B4 _h		BNK80W	8000 _h –9FFF _h RAM write
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B5 _h		BNKA0	A000 _h –BFFF _h RAM under BASIC
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B6 _h		BNKC0	C000 _h –DFFF _h RAM
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B7 _h		BNKC0	E000 _h –FFFF _h RAM under KERNAL
bit	settings	description	
7–0	A ₂₀ –A ₁₃		
D0B8 _h		BNKFD0	Bank for drive emulation (first device)
bit	settings	description	
7–0	A ₂₃ –A ₁₆		
D0B9 _h		BNKFD1	Bank for drive emulation (second device)
bit	settings	description	
7–0	A ₂₃ –A ₁₆		
D0BA _h		BNKRAM	Bank for freezer cartridge RAM
bit	settings	description	
7–0	A ₂₃ –A ₁₆		
D0BB _h		BNKCRT	Bank for freezer cartridge ROM
bit	settings	description	
7–0	A ₂₃ –A ₁₆		
D0BC _h		BNK80R	8000 _h –9FFF _h RAM read or Simple 8K cartridge ROM
bit	settings	description	
7–0	A ₂₀ –A ₁₃	For RAM should be equal to D0B4 _h	
D0BD _h		BNKBAS	A000 _h –BFFF _h BASIC ROM
bit	settings	description	
7–0	A ₂₀ –A ₁₃	See also D0FB _h bit 6	
D0BE _h		BNKCHR	D000 _h –DFFF _h Character ROM
bit	settings	description	
7–0	A ₂₀ –A ₁₃	Only upper 4 KByte of the selected block is used	

D0BF _h	settings	description	BNKCRN	E000 _h -FFFF _h	KERNAL ROM
7-0	A ₂₀ -A ₁₃	See also D0FB _h bit 6			

3.3 Memory Windows

Three memory windows located at D5xx_h, D6xx_h and D7xx_h allow any memory location in the SDRAM of the Chameleon to be accessed. Each of the three windows offer access to 256 continuous memory locations at a time. The offset can be set to any byte address inside the memory, it is not restricted to page or segment boundaries. These windows allow simple access to big tables and offer support for crunchers and other applications that need to index large amounts of memory. It also offers access to memory below kernal and I/O space without banking the memory so interrupts can stay enabled.

Address (Hex)	Address (Dec)	Name	Description
D0A0 _h - D0A3 _h	53408 - 53411		Reserved for future use
D0A4 _h	53412		Address bits A ₇ -A ₀ of memory window at D5xx _h
D0A5 _h	53413		Address bits A ₁₅ -A ₈ of memory window at D5xx _h
D0A6 _h	53414		Address bits A ₂₃ -A ₁₆ of memory window at D5xx _h
D0A7 _h	53415		Address bit A ₂₄ of memory window at D5xx _h
bit	settings		description
7-1	Reserved for address extension, must be set to 0		
0	Address bit A ₂₄		
D0A8 _h	53416		Address bits A ₇ -A ₀ of memory window at D6xx _h
D0A9 _h	53417		Address bits A ₁₅ -A ₈ of memory window at D6xx _h
D0AA _h	53418		Address bits A ₂₃ -A ₁₆ of memory window at D6xx _h
D0AB _h	53419		Address bit A ₂₄ of memory window at D6xx _h
bit	settings		description
7-1	Reserved for address extension, must be set to 0		
0	Address bit A ₂₄		
D0AC _h	53420		Address bits A ₇ -A ₀ of memory window at D7xx _h
D0AD _h	53421		Address bits A ₁₅ -A ₈ of memory window at D7xx _h
D0AE _h	53422		Address bits A ₂₃ -A ₁₆ of memory window at D7xx _h
D0AF _h	53423		Address bit A ₂₄ of memory window at D7xx _h
bit	settings		description
7-1	Reserved for address extension, must be set to 0		
0	Address bit A ₂₄		

4 VGA Output

One of the major features on the Turbo Chameleon Cartridge is the VGA connector. This interface allows rendering of the C64 picture on a VGA monitor in high quality. It doesn't use the original PAL or NTSC output, but generates the picture by monitoring the address and databus of the expansion connector. This results in a crisp and perfect stable picture on the monitor. If compatibility with a stock C64 is not required, the VGA controller can be reprogrammed to provide higher resolutions and more colors.

4.1 VGA Resolution and Sync Registers

Address (Hex)	Address (Dec)	Name	Description
D040 _h			VGA Visual X-size _{7..0}
D041 _h			VGA Visual Y-size _{7..0}
D042 _h			VGA Visual size upper bits
bit	settings		description
7-4	visual Y-size _{11..8}		
3-0	visual X-size _{11..8}		

D043 _h			VGA total X-size _{7..0}
D044 _h			VGA total Y-size _{7..0}
D045 _h			VGA total size upper bits
	bit	settings	description
	7-4	total Y-size _{11..8}	
	3-0	total X-size _{11..8}	
D046 _h			VGA HSync start _{7..0}
D047 _h			VGA HSync end _{7..0}
D048 _h			VGA HSync upper bits
	bit	settings	description
	7-4	HSync end _{11..8}	
	3-0	HSync start _{11..8}	
D049 _h			VGA VSync start _{7..0}
D04A _h			VGA VSync end _{7..0}
D04B _h			VGA VSync upper bits
	bit	settings	description
	7-4	VSync end _{11..8}	
	3-0	VSync start _{11..8}	
D04C _h			Select current object
			Object registers are at D050 _h -D05F _h
D04D _h			First object to render
D04E _h			Last object to render
D04F _h			Polarity and Pixel-clock
	bit	settings	description
	7	VSync polarity	0 = negative sync 1 = positive sync
	6	HSync polarity	0 = negative sync 1 = positive sync
	5	Enable VGA VSync Interrupt	0 = disabled 1 = enabled
	4	VGA VSync Interrupt status	0 = no interrupt 1 = pending
	3-0	Pixel-clock frequency	Interrupt status is cleared on any write to D04F _h 0000 = 25.175 Mhz 0001 = 31.5 Mhz 0010 = Reserved for 36 Mhz 0011 = Reserved for 40 Mhz 0100 = 50 Mhz 0101 = Reserved for 65 Mhz 0110 = Reserved for 75 Mhz 0111 = Reserved for 78.8 Mhz 1000 = 108 Mhz others = Reserved for future use

4.2 Example settings for standard VGA modes

Screen mode	Visual Size W H	Total Size W H	HSync start / end	VSync start / end	Polarity & Pixelclock
640x480 @ 60Hz	640 480	?			H=n / V=p / 25.175
800x600 @ 72Hz	800 600	1040 666	860 / 980	625 / 631	H=p / V=p / 50
1024x768 @ 70Hz	1024 768	1328 806			H=n / V=n / 75
1024x768 @ 75Hz	1024 768	1312 800			H=p / V=p / 78.8
1280x1024 @ 60Hz	1280 1024	1688 1066			H=p / V=p / 108

4.3 Chameleon Object Processor

The COP (Chameleon Object Processor) is a separate processor designed to perform graphic tasks. It can render multiple moving objects to the screen, these objects can take the form of sprites/MOBs or even complete bitmaps (with smooth scrolling in all directions). Objects of different resolutions (pixels can be stretched both horizontally and vertically) and different bit-depths can be combined on the same screen. A object can be configured as a window showing only a part of a larger bitmap. Combining this feature with smooth scroll and byte wise addressing

allows the window to be positioned anywhere on the bitmap. Objects that overlap other objects can have one of their colors set to transparent to show the objects below it.

Programming the COP is done with 19 registers, 16 of these are mapped at D050_h and are used to configure the objects. The register at D04C_h selects one of a possible 256 objects to configure. Registers D04D_h and D04E_h allow selection of a sub-range of objects. Only the objects within this range are rendered to the screen. The drawing order is fixed, an object with lower index number is always behind an object with a higher index number. All other objects outside the range are invisible (and won't use any memory nor object processor bandwidth).

Address (Hex)	Address (Dec)	Name	Description
D050 _h	53328		X position _{7..0}
D051 _h	53329		Y position _{7..0}
D052 _h	53330		Position upper bits
		bit settings description	
	7-4	Y position _{11..8}	
	3-0	X position _{11..8}	
D053 _h	53331		X size _{7..0}
D054 _h	53332		Y size _{7..0}
D055 _h	53333		Size upper bits
		bit settings description	
	7-4	Y size _{11..8}	
	3-0	X size _{11..8}	
D056 _h	53334		Line increment low
D057 _h	53335		Line increment high
D058 _h	53336		Start address bits _{7..0}
D059 _h	53337		Start address bits _{15..8}
D05A _h	53338		Start address bits _{23..16}
D05B _h	53339		Address MSB, Group and Alpha
		bit settings description	
	7	Start address bits ₂₄	
	6-4	Collision group	Selects group for collision detection
	3-0	Alpha	Alpha-blending value in 6% steps (1/16th) 0000 = Fully opaque (100% new) 1111 = 6% of the new color and 94% of background
D05C _h	53340		Palette offset
D05D _h	53341		Smooth scroll (in pixels)
D05E _h	53342		Zoom, stretch and flip
		bit settings description	
	7	Vertical flip	0 = normal 1 = flipped / mirror
	6-4	stretch	000 = normal size 001 = double height pixels 010 = 4x height pixels 011 = 8x height pixels 100 = 16x height pixels others = Reserved for future use
	3	Horizontal flip	0 = normal 1 = flipped / mirror
	2-0	stretch	000 = normal size 001 = double width pixels 010 = 4x width pixels 011 = 8x width pixels 100 = 16x width pixels others = Reserved for future use

D05F _h 53343		Mode selection
bit	settings	description
7	Set clip rectangle	0 = use existing clip rectangle 1 = Set new clip rectangle from object position and dimensions. All following objects will clip to the boundary of this object.
6-5	-	Reserved for future use, must be set to 0
4	Enable color dither	0 = 5 bits color channels (truncated) 1 = 8 bits color channels (dithered)
3	Color keying	0 = object is fully opaque. 1 = color 0 is transparent.
2-0	Color depth	000 = Solid color 001 = 1 bit/pixel, 2 palette colors 010 = 2 bits/pixel, 4 palette colors 011 = 4 bits/pixel, 16 palette colors 100 = 8 bits/pixel, 256 palette colors 101 = 16 bits/pixel, 32768 color mode others = Reserved for future use

4.4 Palette Registers

To support higher color depths on the VGA, a set of registers is added to store custom colors. The 'palette offset' register in the Object-Processor select which of the colors of the palette are being used. The first 32 entries in the color palette are fixed. Entries 32 (020_h) to 287 (11F_h) are software redefinable by using the palette registers (note that entries 271 to 287 are only reachable in 256 color mode).

When bit 0 of configuration register D0FA_h is set, an additional 768 registers become available at memory locations D100_h to D3FF_h. The registers at D1xx_h store the red color intensities. The next 256 registers at D2xx_h store the green intensity of the colors and the last 256 at D3xx_h store the blue intensity value of the RGB triplets. Although the color resolution is limited to 5 bits (bit 7-3), all 8 bits are stored so the palette registers can also be used as 768 bytes of extra memory.

Address (Hex)	Address (Dec)	Name	Description
D100 _h -D1FF _h	53504 -53759	PALRED	256 entry color palette Red intensity
D200 _h -D2FF _h	53760 -54015	PALGRN	256 entry color palette Green intensity
D300 _h -D3FF _h	54016 -54271	PALBLU	256 entry color palette Blue intensity

4.5 Fixed Palette Entries

The first 32 entries in the color palette are fixed. They contain VIC-II and VDC compatible color definitions. Palette entries 0 (000_h) to 15 (00F_h) contain VIC-II compatible colors. Palette entries 16 (010_h) to 31 (01F_h) contain RGBI entries compatible with the VDC chip that is found in Commodore 128 machines. Custom color entries start at palette index 32 (020_h) with the last entry at index 287 (11F_h).

Palette Index	Color (VIC-II)	Palette Index	Color (VDC)
0 (000 _h)	black	16 (010 _h)	black
1 (001 _h)	white	17 (011 _h)	dark gray
2 (002 _h)	red	18 (012 _h)	dark blue
3 (003 _h)	cyan	19 (013 _h)	light blue
4 (004 _h)	purple	20 (014 _h)	dark green
5 (005 _h)	green	21 (015 _h)	light green
6 (006 _h)	blue	22 (016 _h)	dark cyan
7 (007 _h)	yellow	23 (017 _h)	light cyan
8 (008 _h)	orange	24 (018 _h)	dark red
9 (009 _h)	brown	25 (019 _h)	light red
10 (00A _h)	light red	26 (01A _h)	dark purple
11 (00B _h)	dark gray	27 (01B _h)	light purple
12 (00C _h)	mid gray	28 (01C _h)	dark yellow (brown)
13 (00D _h)	light green	29 (01D _h)	yellow
14 (00E _h)	light blue	30 (01E _h)	light gray
15 (00F _h)	light gray	31 (01F _h)	white

5 REU (Ram Expansion Unit) Emulation

The Chameleon can emulate a 17xx !!! REU.

5.1 REU Registers

Address (Hex)	Address (Dec)	Name	Description
DF00 _h	57088	DMAST	REU Status register (read-only, but can be set in configuration mode)
	bit	settings	description
	7	1 = IRQ pending	
	6	1 = End of block	
	5	1 = Fault	Compare operation detected a difference
	4	Size	0 = 128 or 256 KByte 1 = 512 KByte A single bit can't represent all memory sizes. So software should probe for the amount that is really available
	3-0	Version	Always 0000
DF01 _h	57089	DMACMD	REU Command register
	bit	settings	description
	7	1 = Execute	
	6	Reserved	-
	5	1 = Auto load	When autoloading is enabled. The memory pointers and length registers are reloaded at the end of the transfer
	4	FF00 _h flag	0 = Wait for write to FF00 _h before starting transfer 1 = Start immediately when bit 7 becomes set
	3-2	Reserved	-
	1-0	Transfer type	00 = C64 to REU 01 = REU to C64 10 = Swap 11 = Compare / verify
DF02 _h	57090		C64 memory pointer low
DF03 _h	57091		C64 memory pointer high
DF04 _h	57092		REU memory pointer low
DF05 _h	57093		REU memory pointer mid
DF06 _h	57094		REU memory pointer high
DF07 _h	57095		Transfer length low
DF08 _h	57096		Transfer length high

DF09 _h		57097	Interrupt mask register
bit	settings	description	
7	Interrupt enable	1 = enabled	
6	End Of Block mask	1 = interrupt after transfer	
5	Verify mask	1 = interrupt on verify error	
4-0	Reserved	Read as 1	

DF0A _h		57098	Address control register
bit	settings	description	
7	C64 Address control	0 = Increment C64 address 1 = Fix C64 address	
6	REU Address control	0 = Increment REU address 1 = Fix REU address	
5-0	Reserved	Read as 1	

5.2 Blitter extension

The blitter extensions allow the REU to perform rectangular graphic moves in addition to linear arrays. It also extends the "C64 side" addressing space from 64K to 16M allowing larger transfers for blitting in VGA resolution bitmaps. A few additional registers are mapped to previous unused locations to provide access to the extra functionality. The blitter mode is mostly backwards compatible if the additional registers are set to 0, but take note that the wraparound from FFFF_h to 0000_h will not happen if the blitter extensions are activated.

Address (Hex)	Address (Dec)	Name	Description
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6 CPU Turbo/Accelerator

7 Disk Drive Emulation

8 Complete register map

Address (Hex)	Address (Dec)	Name	Description
D040 _h			VGA Visual X-size _{7..0}
D041 _h			VGA Visual Y-size _{7..0}
D042 _h			VGA Visual size upper bits
		bit settings description	
	7-4	visual Y-size _{11..8}	
	3-0	visual X-size _{11..8}	
D043 _h			VGA total X-size _{7..0}
D044 _h			VGA total Y-size _{7..0}
D045 _h			VGA total size upper bits
		bit settings description	
	7-4	total Y-size _{11..8}	
	3-0	total X-size _{11..8}	
D046 _h			VGA HSync start _{7..0}
D047 _h			VGA HSync end _{7..0}
D048 _h			VGA HSync upper bits
		bit settings description	
	7-4	HSync end _{11..8}	
	3-0	HSync start _{11..8}	
D049 _h			VGA VSync start _{7..0}
D04A _h			VGA VSync end _{7..0}
D04B _h			VGA VSync upper bits
		bit settings description	
	7-4	VSynch end _{11..8}	
	3-0	VSynch start _{11..8}	

D04C_h Select current object
 Object registers are at D050_h-D05F_h
 D04D_h First object to render
 D04E_h Last object to render
 D04F_h Polarity and Pixel-clock

bit	settings	description
7	VSync polarity	0 = negative sync 1 = positive sync
6	HSync polarity	0 = negative sync 1 = positive sync
5	Enable VGA VSync Interrupt	0 = disabled 1 = enabled
4	VGA VSync Interrupt status	0 = no interrupt 1 = pending
3-0	Pixel-clock frequency	Interrupt status is cleared on any write to D04F _h 0000 = 25.175 Mhz 0001 = 31.5 Mhz 0010 = Reserved for 36 Mhz 0011 = Reserved for 40 Mhz 0100 = 50 Mhz 0101 = Reserved for 65 Mhz 0110 = Reserved for 75 Mhz 0111 = Reserved for 78.8 Mhz 1000 = 108 Mhz others = Reserved for future use

D050_h 53328 X position_{7..0}
 D051_h 53329 Y position_{7..0}
 D052_h 53330 Position upper bits

bit	settings	description
7-4	Y position _{11..8}	
3-0	X position _{11..8}	

D053_h 53331 X size_{7..0}
 D054_h 53332 Y size_{7..0}
 D055_h 53333 Size upper bits

bit	settings	description
7-4	Y size _{11..8}	
3-0	X size _{11..8}	

D056_h 53334 Line increment low
 D057_h 53335 Line increment high
 D058_h 53336 Start address bits_{7..0}
 D059_h 53337 Start address bits_{15..8}
 D05A_h 53338 Start address bits_{23..16}
 D05B_h 53339 Address MSB, Group and Alpha

bit	settings	description
7	Start address bits ₂₄	
6-4	Collision group	Selects group for collision detection
3-0	Alpha	Alpha-blending value in 6% steps (1/16th) 0000 = Fully opaque (100% new) 1111 = 6% of the new color and 94% of background

D05C_h 53340 Palette offset
 D05D_h 53341 Smooth scroll (in pixels)
 D05E_h 53342 Zoom, stretch and flip

bit	settings	description
7	Vertical flip	0 = normal 1 = flipped / mirror
6-4	stretch	000 = normal size 001 = double height pixels 010 = 4x height pixels 011 = 8x height pixels 100 = 16x height pixels others = Reserved for future use
3	Horizontal flip	0 = normal 1 = flipped / mirror
2-0	stretch	000 = normal size 001 = double width pixels 010 = 4x width pixels 011 = 8x width pixels 100 = 16x width pixels others = Reserved for future use

D05F _h 53343			Mode selection
bit	settings	description	
7	Set clip rectangle	0 = use existing clip rectangle 1 = Set new clip rectangle from object position and dimensions. All following objects will clip to the boundary of this object.	
6-5	-	Reserved for future use, must be set to 0	
4	Enable color dither	0 = 5 bits color channels (truncated) 1 = 8 bits color channels (dithered)	
3	Color keying	0 = object is fully opaque. 1 = color 0 is transparent.	
2-0	Color depth	000 = Solid color 001 = 1 bit/pixel, 2 palette colors 010 = 2 bits/pixel, 4 palette colors 011 = 4 bits/pixel, 16 palette colors 100 = 8 bits/pixel, 256 palette colors 101 = 16 bits/pixel, 32768 color mode others = Reserved for future use	
D0A0 _h -D0A3 _h	53408-53411	Reserved for future use	
D0A4 _h	53412	Address bits A ₇ -A ₀ of memory window at D5xx _h	
D0A5 _h	53413	Address bits A ₁₅ -A ₈ of memory window at D5xx _h	
D0A6 _h	53414	Address bits A ₂₃ -A ₁₆ of memory window at D5xx _h	
D0A7 _h	53415	Address bit A ₂₄ of memory window at D5xx _h	
bit	settings	description	
7-1	Reserved for address extension, must be set to 0		
0	Address bit A ₂₄		
D0A8 _h	53416	Address bits A ₇ -A ₀ of memory window at D6xx _h	
D0A9 _h	53417	Address bits A ₁₅ -A ₈ of memory window at D6xx _h	
D0AA _h	53418	Address bits A ₂₃ -A ₁₆ of memory window at D6xx _h	
D0AB _h	53419	Address bit A ₂₄ of memory window at D6xx _h	
bit	settings	description	
7-1	Reserved for address extension, must be set to 0		
0	Address bit A ₂₄		
D0AC _h	53420	Address bits A ₇ -A ₀ of memory window at D7xx _h	
D0AD _h	53421	Address bits A ₁₅ -A ₈ of memory window at D7xx _h	
D0AE _h	53422	Address bits A ₂₃ -A ₁₆ of memory window at D7xx _h	
D0AF _h	53423	Address bit A ₂₄ of memory window at D7xx _h	
bit	settings	description	
7-1	Reserved for address extension, must be set to 0		
0	Address bit A ₂₄		
D0B0 _h		BNK00	0000 _h -1FFF _h RAM
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B1 _h		BNK20	2000 _h -3FFF _h RAM
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B2 _h		BNK40	4000 _h -5FFF _h RAM
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B3 _h		BNK60	6000 _h -7FFF _h RAM
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B4 _h		BNK80W	8000 _h -9FFF _h RAM write
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B5 _h		BNKA0	A000 _h -BFFF _h RAM under BASIC
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B6 _h		BNKC0	C000 _h -DFFF _h RAM
bit	settings	description	
7-0	A ₂₀ -A ₁₃		
D0B7 _h		BNKC0	E000 _h -FFFF _h RAM under KERNAL
bit	settings	description	
7-0	A ₂₀ -A ₁₃		

D0B8 _h			BNKFD0	Bank for drive emulation (first device)
bit	settings	description		
7-0	A ₂₃ -A ₁₆			
D0B9 _h			BNKFD1	Bank for drive emulation (second device)
bit	settings	description		
7-0	A ₂₃ -A ₁₆			
D0BA _h			BNKRAM	Bank for freezer cartridge RAM
bit	settings	description		
7-0	A ₂₃ -A ₁₆			
D0BB _h			BNKCRT	Bank for freezer cartridge ROM
bit	settings	description		
7-0	A ₂₃ -A ₁₆			
D0BC _h			BNK80R	8000 _h -9FFF _h RAM read or Simple 8K cartridge ROM
bit	settings	description		
7-0	A ₂₀ -A ₁₃	For RAM should be equal to D0B4 _h		
D0BD _h			BNKBAS	A000 _h -BFFF _h BASIC ROM
bit	settings	description		
7-0	A ₂₀ -A ₁₃	See also D0FB _h bit 6		
D0BE _h			BNKCHR	D000 _h -DFFF _h Character ROM
bit	settings	description		
7-0	A ₂₀ -A ₁₃	Only upper 4 KByte of the selected block is used		
D0BF _h			BNKKRN	E000 _h -FFFF _h KERNAL ROM
bit	settings	description		
7-0	A ₂₀ -A ₁₃	See also D0FB _h bit 6		
D0F0 _h		53488	CFG???	Reserved
D0F1 _h		53489	CFG???	Reserved
D0F2 _h		53490	CFGVIC	VIC-II Emulation Config
bit	settings			description
7	VIC-II Read Enable			0 = Off 1 = Perform memory accesses for VIC-II
6-5	VIC-II update framebuffer			00 = No update, there is no output from VIC-II on the VGA 01 = VIC-II writes to VGA framebuffer at 2097152-2228223 (200000 _h -21FFFF _h) 10 = VIC-II writes to VGA framebuffer at 4194304-4325375 (400000 _h -41FFFF _h) 11 = VIC-II writes to VGA framebuffer at 6291456-6422527 (600000 _h -61FFFF _h)
4	reserved, must be 0			-
3	VIC-II emulation error (or hardware problem)			0 = VGA emulation in sync. with VIC-II chip 1 = Error, VGA and VIC-II chip not in sync. This bit is read-only and has a value in cartridge mode only.
2-0	VIC-II type			000 = PAL (63 columns, 312 lines) 001 = Reserved 010 = NTSC (65 columns, 263 lines) 011 = Old-NTSC (64 columns, 262 lines) 1xx = Reserved These bits are read-only in cartridge mode. They can be changed in standalone mode and on the C-One.
D0F3 _h		53491		Reserved
D0F4 _h		53492	CFGTUR	Turbo configuration
bit	settings		description	
7	Turbo Enable			0 = 1 Mhz mode 1 = Turbo mode active
6	Turbo switch			0 = Manual setting 1 = Turbo mode is switchable
5	VIC-II turbo bit			0 = Off 1 = "Turbo Enable" is mirrored at bit 0 of D030 _h
4-0	reserved, must be 0			-
D0F5 _h		53493		Reserved

D0F6 _h	53494	CFGREU	REU (Ram Expansion Unit) Emulation Config
bit	settings	description	
7	1 = Enable REU	Enable REU emulation and activate registers at DF00 _h –DF0A _h .	
6	1 = Enable Blitter Extensions	Extra registers are added at DF0B _h –DF0F _h that enhance the REU so it can perform simple bit-bit functions.	
5	reserved, must be 0	–	
4	reserved, must be 0	–	
3	reserved, must be 0	–	
2–0	REU memory size	000 = 128 KByte 001 = 256 KByte 010 = 512 KByte 011 = 1 MByte 100 = 2 MByte 101 = 4 MByte 110 = 8 MByte 111 = 16 MByte (Not available on C-One, selects 8 MByte)	
D0F7 _h	53495	CFGCIA	CIA, keyboard and IEC configuration
bit	settings	description	
7	IEC port	0 = Chameleon IEC bus connected to virtual CIAs 1 = Chameleon IEC bus is disconnected By setting this bit, the Chameleon IEC bus is disconnected from the C64 side. In this mode the Chameleon can function as a 1541 drive emulator. This feature is not available on the C-One due to a hardware limitation.	
6-2	Reserved	–	
1	CIA-2 emulation	0 = Old 1 = Type A This bit has no effect in cartridge mode	
0	CIA-1 emulation	0 = Old 1 = Type A This bit has no effect in cartridge mode	
D0F8 _h	53496	CFGFD0	Drive emulation
bit	settings	description	
7	Enable virtual-drive CPU	0 = drive cpu stopped 1 = drive cpu running	
6	Reset virtual-drive CPU	0 = normal operation 1 = drive reset (bit 7 must be 1 for proper reset)	
5–2	Reserved, must be 0	–	
1–0	Drive ID jumpers	00 = drive device id is 8 01 = drive device id is 9 10 = drive device id is 10 11 = drive device id is 11	
D0F9 _h	53497	CFGFD1	Reserved for second drive
bit	settings	description	
7	Enable virtual-drive CPU	0 = drive cpu stopped 1 = drive cpu running	
6	Reset virtual-drive CPU	0 = normal operation 1 = drive reset (bit 7 must be 1 for proper reset)	
5–2	Reserved, must be 0	–	
1–0	Drive ID jumpers	00 = drive device id is 8 01 = drive device id is 9 10 = drive device id is 10 11 = drive device id is 11	
D0FA _h	53498	CFGREG	Enable VGA, palette and window registers
bit	settings	description	
7	Enable memory window at D7xx _h	0 = standard function (SID mirror) 1 = Memory window	
6	Enable memory window at D6xx _h	0 = standard function (SID mirror) 1 = Memory window	
5	Enable memory window at D5xx _h	0 = standard function (SID mirror) 1 = Memory window	
4	reserved, must be 0	–	
3	Palette Registers Enable	0 = VIC-II chip mirrors at D100 _h –D3FF _h 1 = Palette registers are at D100 _h –D3FF _h	
2	Enable Bank Registers	0 = VIC-II chip mirrors at D0B0 _h –D0BF _h 1 = Bank and MMU at D0B0 _h –D0BF _h	
1	Enable memory window address registers	0 = VIC-II chip mirrors at D0A0 _h –D0AF _h 1 = Memory window addresses at D0A0 _h –D0AF _h	
0	Enable VGA Controller Registers	0 = VIC-II chip mirrors at D040 _h –D07F _h 1 = VGA registers at D040 _h –D07F _h	

D0FB _h	53499	CFGBOT	Boot control register
bit	settings	description	
7	Boot Image	If bit 7 of this register is zero, a special bootrom contained in the FPGA image is mapped to E000 _h -FFFF _h or 8000 _h -9FFF _h depending on cartridge revision. This bootrom is responsible for initializing the cartridge at power-up. 0 = Bootrom mapped into C64 memory space 1 = Normal operation	
6	ROM source	0 = C64 original Basic and Kernal ROMs are used 1 = All memory and ROMs are banked with D0B0 _h -D0BF _h This bit is only functional in cartridge mode. In standalone mode and on the C-One this bit should always be set. Note that the character ROM is always emulated and never the C64 original.	
5-0	reserved, must be 0	-	
D0FC _h	53500	CFG???	Reserved
D0FD _h	53501	CFGDIS	A write (any value) leaves configuration mode
D0FE _h	53502	CFGENA	Write 42 (2A _h) to enter configuration mode
D0FF _h	53503	CFGDIS	A write (any value) leaves configuration mode
D100 _h	-D1FF _h	53504 -53759	PALRED 256 entry color palette Red intensity
D200 _h	-D2FF _h	53760 -54015	PALGRN 256 entry color palette Green intensity
D300 _h	-D3FF _h	54016 -54271	PALBLU 256 entry color palette Blue intensity
DF00 _h	57088	DMAST	REU Status register (read-only, but can be set in configuration mode)
bit	settings	description	
7	1 = IRQ pending		
6	1 = End of block		
5	1 = Fault	Compare operation detected a difference	
4	Size	0 = 128 or 256 KByte 1 = 512 KByte A single bit can't represent all memory sizes. So software should probe for the amount that is really available	
3-0	Version	Always 0000	
DF01 _h	57089	DMACMD	REU Command register
bit	settings	description	
7	1 = Execute		
6	Reserved	-	
5	1 = Auto load	When autoloading is enabled. The memory pointers and length registers are reloaded at the end of the transfer	
4	FF00 _h flag	0 = Wait for write to FF00 _h before starting transfer 1 = Start immediately when bit 7 becomes set	
3-2	Reserved	-	
1-0	Transfer type	00 = C64 to REU 01 = REU to C64 10 = Swap 11 = Compare / verify	
DF02 _h	57090	C64 memory pointer low	
DF03 _h	57091	C64 memory pointer high	
DF04 _h	57092	REU memory pointer low	
DF05 _h	57093	REU memory pointer mid	
DF06 _h	57094	REU memory pointer high	
DF07 _h	57095	Transfer length low	
DF08 _h	57096	Transfer length high	
DF09 _h	57097	Interrupt mask register	
bit	settings	description	
7	Interrupt enable	1 = enabled	
6	End Of Block mask	1 = interrupt after transfer	
5	Verify mask	1 = interrupt on verify error	
4-0	Reserved	Read as 1	
DF0A _h	57098	Address control register	
bit	settings	description	
7	C64 Address control	0 = Increment C64 address 1 = Fix C64 address	
6	REU Address control	0 = Increment REU address 1 = Fix REU address	
5-0	Reserved	Read as 1	